a transparent first metal layer and a transparent second metal layer on the insulator.

43. (New) The device of claim 42, further comprising a plurality of thin film transistors at crossing points of the gate and data bus lines.

44. (New) The device of claim 43, wherein each of the thin film transistors include:

a gate electrode on the first substrate;

a semiconductor layer on the gate electrode; and

source and drain electrodes on the semiconductor layer.

45. (New) The device of claim 44, wherein the transparent first metal layer is connected to the source and drain electrodes.

46. (New) The device of claim 42, wherein the transparent second metal layer is connected to the common line.

47. (New) The device of claim 42, wherein the common line and the transparent first metal layer form a first storage capacitor.

48. (New) The device of claim 42, wherein the transparent first metal layer and the transparent second metal layer form a second storage capacitor.

49. (New) The device of claim 42, wherein the transparent first metal layer includes a data electrode and the transparent second metal layer includes a common electrode.

50. (New) The device of claim 42, wherein the transparent first and second metal layers include indium tin oxide.

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51. (New) The device of claim 42, further comprising a first alignment layer on the first substrate.

52. (New) The device of claim 51, wherein the first alignment layer includes one of polyimide, polyamide, polyvinylcinnamate, and polysiloxanecinnamate.

53. (New) The device of claim 42, further comprising:

a black matrix layer on the second substrate;

a color filter on the black matrix layer; and

a liquid crystal layer between the first and second substrates.

54. (New) The device of claim 42, further comprising a second alignment layer on the second substrate.

55. (New) The device of claim 54, wherein the second alignment layer includes one of polyimide, polyamide, polyvinylcinnamate, and polysiloxanecinnamate.

56. (New) A method of forming an in-plane switching liquid crystal display device, comprising:

forming first and second substrates;

forming a plurality of gate and data bus lines on the first substrate, the gate lines being crossed with the data bus lines;

forming a common line in parallel to any one of the gate lines and the data bus lines on the first substrate;

forming an insulator on the first substrate; and

a transparent first metal layer and a transparent second metal layer on the insulator.

57. (New) The method of claim 56, further comprising forming a plurality of thin film transistors at crossing points of the gate and data bus lines.

58. (New) The method of claim 57, wherein each of the thin film transistors include:

a gate electrode on the first substrate;

a semiconductor layer on the gate electrode; and

source and drain electrodes on the semiconductor layer.

59. (New) The method of claim 58, wherein the transparent first metal layer is connected to the source and drain electrodes.

60. (New) The method of claim 56, wherein the transparent second metal layer is connected to the common line.

61. (New) The method of claim 56, wherein the common line and the transparent first metal layer form a first storage capacitor.

62. (New) The method of claim 56, wherein the transparent first metal layer and the transparent second metal layer form a second storage capacitor.

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63. (New) The method of claim 56, wherein the transparent first metal layer includes a data electrode and the transparent second metal layer includes a common electrode.

64. (New) The method of claim 56, wherein the transparent first and second metal layers include indium tin oxide.

65. (New) The method of claim 56, further comprising forming a first alignment layer on the first substrate.

66. (New) The method of claim 65, wherein the first alignment layer includes one of polyimide, polyamide, polyvinylcinnamate, and polysiloxanecinnamate.

67. (New) The method of claim 56, further comprising:

forming a black matrix layer on the black matrix layer;

forming a color filter layer on the black matrix layer; and

forming a liquid crystal layer between the first and second substrates.